IN THE CLAIMS:

Claims 14 and 19 have been amended herein. All of the pending claims 1 through 19 are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as amended.

Listing of Claims:

1. (Previously presented) A manufacturing process having data for integrated circuit devices comprising:

storing data and a substantially unique identification code of each integrated circuit device of the integrated circuit devices at one of at probe testing of the integrated circuit devices and after probe testing of the integrated circuit devices, the data indicating a process flow within the manufacturing process for each integrated circuit device of the integrated circuit devices, storing data comprising:

storing the substantially unique identification code of each integrated circuit device of the integrated circuit devices and a die location on an electronically stored wafer map for each integrated circuit device;

reading the substantially unique identification code of each integrated circuit device of the integrated circuit devices;

evaluating the data for each integrated circuit device of the integrated circuit devices to the data for manufacturing process data stored for each integrated circuit device;

identifying integrated circuit devices having a process flow within the manufacturing process different from the process flow of the data stored of the integrated circuit devices; and

directing the integrated circuit devices identified as having a process flow within the manufacturing process different from the process flow of the data stored of the integrated circuit devices to another process.

2. (Previously presented) The process of claim 1, wherein storing data comprises storing data at a probe.

3. (Previously presented) The process of claim 1, wherein storing data comprises storing data and the substantially unique identification code of each integrated circuit device of the integrated circuit devices to indicate each integrated circuit device of the integrated circuit devices comprises one of a good integrated circuit device and a bad integrated circuit device.

4. (Previously presented) The process of claim 1, wherein reading the substantially unique identification code of each integrated circuit device of the integrated circuit devices comprises electrically retrieving a unique fuse identification programmed into each integrated circuit device of the integrated circuit devices.

5. (Previously presented) The process of claim 1, wherein reading the substantially unique identification code of each integrated circuit device of the integrated circuit devices comprises optically reading a unique identification code on each integrated circuit device of the integrated circuit devices.

6. (Previously presented) The process of claim 5, wherein optically reading the unique identification code on each integrated circuit device of the integrated circuit devices comprises optically reading a unique laser fuse identification programmed into each integrated circuit device of the integrated circuit devices.

7. (Previously presented) The process of claim 1, wherein reading the substantially unique identification code of each integrated circuit device of the integrated circuit devices comprises reading the substantially unique identification code of each integrated circuit device of the integrated circuit devices at an opens/shorts test in the manufacturing process.

8. (Previously presented) The process of claim 1, wherein the stored data and the substantially unique identification code of each integrated circuit device of the integrated circuit devices are accessed by accessing the stored data and the substantially unique identification code of each integrated circuit device of the integrated circuit devices at an opens/shorts test in the manufacturing process.

9. (Previously presented) The process of claim 8, wherein evaluating the data comprises evaluating the data for each integrated circuit device of the integrated circuit devices to identify any bad integrated circuit devices having undergone an assembly procedure within the manufacturing process.

10. (Previously presented) The process of claim 9, wherein evaluating the data comprises evaluating the data at an opens/shorts test in the manufacturing process.

11. (Previously presented) The process of claim 1, wherein directing the integrated circuit devices identified as having a process flow within the manufacturing process different from the process flow of the stored data of the integrated circuit devices to another process comprises discarding any integrated circuit device identified as having a process flow within the manufacturing process different from the process flow of the stored data.

12. (Previously presented) The process of claim 1, wherein directing occurs before a back-end test procedure within the manufacturing process.

13. (Previously presented) The process of claim 1, further comprising assembling the integrated circuit devices into packaged integrated circuit devices after storing data and before reading the substantially unique identification code of each integrated circuit device of the integrated circuit devices.

14. (Currently amended) A method of manufacturing integrated circuit devices comprising:

providing a plurality of semiconductor wafers, each semiconductor wafer having a plurality of integrated circuit devices thereon, the plurality of integrated circuit devices comprising:

integrated circuit devices selected from a group comprising Dynamic Random Access Memory (DRAM) devices, Static Random Access Memory (SRAM) devices, synchronous DRAM (SDRAM) devices, and processor devices;

storing a substantially unique identification code in each integrated circuit device of the plurality of integrated circuit devices on each semiconductor wafer of the plurality of semiconductor wafers;

storing data and the substantially unique identification code of each integrated circuit device of the plurality of integrated circuit devices indicating manufacturing processes for each integrated circuit device of the plurality of integrated circuit devices at one of probe testing and after probe testing of the plurality of integrated circuit devices;

separating each integrated circuit device of the plurality of integrated circuit devices on each semiconductor wafer of the plurality of semiconductor wafers to form an integrated circuit device of a plurality of integrated circuit devices;

assembling each integrated circuit device of the plurality of integrated circuit devices into an integrated circuit device assembly;

reading the substantially unique identification code of each integrated circuit device of the integrated circuit device assemblies;

evaluating data for each integrated circuit device of the integrated circuit device assemblies identifying any integrated circuit devices having undergone any manufacturing process different from the indicated manufacturing processes of the stored data for each integrated circuit device;

subjecting to further processing the integrated circuit devices of the plurality of integrated circuit devices identified as having undergone a manufacturing process different from the indicated manufacturing processes of its stored data; and

back-end testing integrated circuit devices not subjected to further processing.

15. (Previously presented) The method of claim 14, further comprising programming each integrated circuit device of the plurality of integrated circuit devices on each semiconductor wafer of the plurality of semiconductor wafers to permanently store a unique fuse identification.

16. (Previously presented) The method of claim 15, wherein programming each integrated circuit device of the plurality of integrated circuit devices on each semiconductor wafer of the plurality of semiconductor wafers to permanently store the unique fuse identification comprises programming at least one of fuses and anti-fuses in each integrated circuit device of the plurality of integrated circuit devices on each semiconductor wafer of the plurality of semiconductor wafers to permanently store the unique fuse identification.

17. (Previously presented) The method of claim 14, wherein assembling each integrated circuit device of the plurality of integrated circuit devices into an integrated circuit device assembly comprises:

picking each integrated circuit device of the plurality of integrated circuit devices from its semiconductor wafer of the plurality of semiconductor wafers;

placing each integrated circuit device of the plurality of integrated circuit devices onto an epoxy-coated bonding site of one of a plurality of lead frames;

curing the epoxy on the bonding site of each one of the plurality of lead frames;

wire bonding each integrated circuit device of the plurality of integrated circuit devices to its associated lead frame;

injection molding each integrated circuit device of the plurality of integrated circuit devices and its associated lead frame to form one of a plurality of integrated circuit device packages, each having projecting leads;

deflashing the projecting leads of each integrated circuit device package of the plurality of integrated circuit device packages;

curing each integrated circuit device package of the plurality of integrated circuit device packages;

electroplating the projecting leads of each integrated circuit device package of the plurality of integrated circuit device packages;

singulating each integrated circuit device package of the plurality of integrated circuit device packages into one of a plurality of discrete integrated circuit devices; and

testing each discrete integrated circuit device of the plurality of discrete integrated circuit devices for opens and shorts.

18. (Previously presented) The method of claim 14, wherein assembling each integrated circuit device of the plurality of integrated circuit devices into an integrated circuit device assembly comprises assembling each integrated circuit device of the plurality of integrated circuit devices into an integrated circuit device selected from a group comprising a wire bond/lead frame integrated circuit device, a Chip-On-Board (COB) integrated circuit device, a flip-chip integrated circuit device, and a Tape-Automated Bonding (TAB) integrated circuit device.

19. (Currently amended) A method of manufacturing Multi-Chip Modules comprising:

providing a plurality of integrated circuit devices on a semiconductor wafer of a plurality of semiconductor wafers;

storing a substantially unique identification code in each integrated circuit device of the plurality of integrated circuit devices on each semiconductor wafer of the plurality of semiconductor wafers at one of probe testing and after probe testing;

storing data and the substantially unique identification code of each integrated circuit device of the plurality of integrated circuit devices indicating desired manufacturing processes for each integrated circuit device of the plurality of integrated circuit devices;

separating each integrated circuit device of the plurality of integrated circuit devices on each semiconductor wafer of a plurality of semiconductor wafers from each semiconductor wafer to form one of a plurality of integrated circuit devices;

assembling one or more integrated circuit devices of the plurality of integrated circuit devices into each of a plurality of multi-chip modules, the plurality of multi-chip modules selected from a group comprising Single In-Line Memory Modules ~~(SIMM's)~~ (SIMMs) and Dual In-line Memory Modules ~~(DIMM's);~~ (DIMMs);

reading the substantially unique identification code of each integrated circuit device of the plurality of integrated circuit devices in each of the plurality of multi-chip modules;

evaluating data for each integrated circuit device of the plurality of integrated circuit devices in each of the plurality of multi-chip modules identifying any multi-chip modules having integrated circuit devices having undergone a manufacturing process that is different from the desired manufacturing processes;

redirecting any multi-chip modules identified as having integrated circuit devices having undergone the manufacturing process that is different from the desired manufacturing processes; and

back-end testing any nonredirected multi-chip modules.